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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,507	07/24/2003	Son Ho	MP0390	1965

26703 7590 02/23/2010

HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 200
TROY, MI 48098

EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
02/23/2010	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SON HO, KEVIN TONTHAT, and HAI VAN

Appeal 2009-005314
Application 10/626,507
Technology Center 2100

Decided: February 23, 2010

Before JOSEPH L. DIXON, CAROLYN D. THOMAS, and
JAMES R. HUGHES, *Administrative Patent Judges*.

DIXON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-28, 44-63, and 79-105. Claims 29-43, 64-78, and 106-120 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We Affirm.

I. STATEMENT OF THE CASE

The Invention

The invention at issue on appeal relates to a method and apparatus for operating and controlling a line cache (Spec. 1).

The Illustrative Claim

Claim 1, an illustrative claim, reads as follows:

> 1. A line cache control system that controls data flow between a line cache, a first central processing unit (CPU) and first and second memory devices, comprising:
>
> a first line cache interface that is associated with the first CPU, that receives a first program read request from the first CPU and that generates a first address from said first program read request;
>
> a first memory interface that communicates with the first memory device;
>
> a second memory interface that communicates with the second memory device;
>
> a line cache that receives a second address that is based on the first address and includes a memory select portion; and

a switch that receives the second address and that selectively connects said line cache to one of said first and second memory interfaces based on the memory select portion,

wherein when said line cache receives said second address, said line cache compares said second address to stored addresses in said line cache, returns data associated with said second address if a match occurs, and retrieves data from one of the first and second memory devices if a miss occurs, and

wherein said switch includes a plurality of selectors that each receive the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively, based on the second address.

The References

The Examiner relies on the following references as evidence of unpatentability:

Bryant	US 4,008,460	Feb. 15, 1977
Taylor	US 5,699,551	Dec. 16, 1997
Alexander	US 6,131,155	Oct. 10, 2000
Zaidi	US 6,601,126 B1	Jul. 29, 2003
Barroso	US 6,725,334 B2	Apr. 20, 2004
Ebner	US 6,928,525 B1	Aug. 9, 2005
Jeddeloh	US 7,133,972 B2	Nov. 7, 2006 (filed Jun. 7, 2002)

Jim Handy, *The Cache Memory Book*, pp. 14-15 and 42-47 (Academic Press, 2nd ed. 1998) (hereafter "Handy").

Alexander V. Veidenbaum, et al., *Adapting Cache line Size to Application Behavior*, Proc. 13th Int'l Conference on Supercomputing, pp. 145-154 (ACM, 1999) (hereafter "Veidenbaum").

The Rejections

The following rejections are before us for review:

Claims 1-5, 11, 13-15, 20, 44-48, 50, 52-54, 79-83, 89, 91, 92, and 97 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Zaidi, Handy, Taylor, and Jeddeloh.

Claims 16-18, 55-57, and 93-95 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Zaidi, Handy, Taylor, Bryant, and Jeddeloh.

Claims 6, 21-24, 28, 49, 59-63, 84, 98-101, and 105 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Zaidi, Handy, Taylor, Barroso, and Jeddeloh.

Claims 7-10, 25-27, 85-88, and 102-104 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Zaidi, Handy, Taylor, Barroso, Alexander, and Jeddeloh.

Claims 19, 58, and 96 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Zaidi, Handy, Taylor, Barroso, Veidenbaum, and Jeddeloh.

Claims 12, 51, and 90 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Zaidi, Handy, Taylor, Barroso, Ebner, and Jeddeloh.

II. ISSUE

Have the Appellants shown that the Examiner erred in finding that the combination of Zaidi, Handy, Taylor, and Jeddeloh teaches or fairly suggests "switch includes a plurality of selectors that each receive the second address

and each select between first and second sets of signals relating to the first and second memory devices, respectively, based on the second address," as recited in claim 1?

III. PRINCIPLES OF LAW

Prima Facie Case of Unpatentability

Appellants have the opportunity on appeal to the Board of Patent Appeals and Interferences (BPAI) to demonstrate error in the Examiner's position. *In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (citing *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998).

Claim Interpretation

The claim construction analysis begins with the words of the claim. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Absent an express intent to impart a novel meaning to a claim term, the words take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art. *Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 (Fed. Cir. 2003).

"Giving claims their broadest reasonable construction 'serves the public interest by reducing the possibility that claims, finally allowed, will be given broader scope than is justified.'" *In re American Academy of Science Tech Center*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (quoting *In re Yamamoto*, 740 F.2d 1569, 1571 (Fed. Cir. 1984)).

Obviousness

"Obviousness is a question of law based on underlying findings of fact." *In re Kubin*, 561 F.3d 1351, 1355 (Fed. Cir. 2009). The underlying factual inquiries are: (1) the scope and content of the prior art, (2) the differences between the prior art and the claims at issue, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations of nonobviousness. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (citation omitted).

IV. FINDINGS OF FACT

The following findings of fact (FFs) are supported by a preponderance of the evidence.

Zaidi

1. Zaidi discloses utilizing a switching device or memory controller, and "[p]oint-to-point signals and ***multiplexing*** are used instead of shared tri-stated lines to deliver higher performance" (col. 25, ll. 33-40 (emphasis added); Fig. 26).

2. Zaidi further discloses providing an address to a switching device or memory controller to allow the switching device to connect with the requested port or memory bank:

> As with a standard memory controller, any DMA peripherals and CPUs supply a request and an address to a switched channel memory controller. However, the address includes both the port, device or memory band address, and the requested memory location address. Once a requested port, device or bank is free, the requesting DMA or CPU is granted access and can begin transferring data.

(Col. 23, ll. 22-39; Figs. 20-23).

Jeddeloh

3. Jeddeloh discloses a memory hub 130 includes a switch 160 coupled to three memory interfaces 170a-c, which are in turn coupled to the system memory device 140a-c (col. 4, ll. 8-17, 30-36; Fig. 3). The switch 160 may be a set of multiplexers (col. 4, ll. 61-62, col. 6, ll. 16-17).

V. ANALYSIS

The Examiner sets forth a detailed explanation of a reasoned conclusion of unpatentability in the Examiner's Answer. Therefore, we look to Appellants' Briefs to show error therein. *See In re Kahn*, 441 F.3d at 985-86.

Grouping of Claims

The Appellants have elected to argue independent claims 1, 12, 16, 19, 21, 44, 51, 55, 58, 59, 79, 90, 94, 96, and 98 together as a group (App. Br. 9). Therefore, we select independent claim 1 as the representative claim for this group, and we will address the Appellants' arguments with respect thereto. 37 C.F.R. § 41.37(c)(1)(vii). *See also In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987).

35 U.S.C. § 103(a) rejections

With respect to claim 1, the Appellants contend that Zaidi fails to teach the claimed switch including a plurality of selectors that receive the

second address and select between a sets of signals based on the second address (App. Br. 10; Reply Br. 3). The Appellants further contend that "the MAC 140 does not necessarily include a plurality of selectors as Appellants' claims recite" because the MAC 140 receives all data over a shared memory bus 104 (Reply Br. 3).

We disagree with the Appellant's contentions. We start our analysis with claim construction. We broadly yet reasonably construe the claim limitation "selector" as either a device selecting signals or a multiplexer. We also broadly yet reasonably construe the claim limitation "second address" as any address received by the switching device.

We find Zaidi teaches that a switching device for memory controlling utilizes multiplexing instead of shared tri-state lines (FF 1). Thus, the multiplexer(s) must be used in the switching device, which can be read on the argued limitation based on our claim construction. We find Zaidi further teaches providing an address to the switching device including the requested device address and requested memory location in order to transfer data (FF 2). Under our claim construction, the requested device address such as the address of a port or memory bank can be read on the limitation of claim 1 of the "second address." The switching device will switch a channel based on the address to allow the data transfer.

The Appellants further contend that claim 1 is allowable because Jeddeloh fails to teach that "switch 160 . . . includes a plurality of selectors that select between sets of signals based on a second address" (App. Br. 14; Reply Br. 4).

We disagree with the Appellant's contention. We find Jeddeloh

teaches that a switcher 160 may be a set of multiplexers, and thus, a plurality of selectors under our claim construction (FF 3).

The Supreme Court noted that an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418. We conclude that utilizing a multiplexer in a switching device for memory controlling would have been within the skill in the art, as evidenced by Zaidi and/or Jeddeloh. Furthermore, it would have been obvious at the time of invention to use the art recognized use of a multiplexer in a switching device of Zaidi or Jeddeloh that is controlled by the second address, and would predictably reduce the system and verification time--a result Zaidi teaches to be desirable. We, therefore, find that combining well-known elements of utilizing a multiplexer in a switching device for memory controlling with the well-known technique of using the address controlling the switching device for data transferring taught by Zaidi is nothing more than a "predictable use of prior art elements according to their established functions." *KSR*, 550 U.S. at 417.

Accordingly, we sustain the Examiner's obviousness rejection of independent claim 1. We also sustain the Examiner's obviousness rejection of independent claims 12, 16, 19, 21, 44, 51, 55, 58, 59, 79, 90, 94, 96, and 98, which are argued as the same group. We further sustain the Examiner's obviousness rejection of dependent claims 2-11, 13-15, 17, 18, 20, 22-28, 45-50, 52-54, 56, 57, 60-63, 80-89, 91-93, 95, 97, and 99-105, which have not been separately argued, and fall with their base claims. 37 C.F.R.

§ 41.37(c)(1)(vii). *See also In re Nielson*, 816 F.2d at 1572.

VI. CONCLUSION

Therefore, based on our consideration of the totality of the record before us, we have weighed the evidence of obviousness found in the combined teachings of the applied references with Appellants' countervailing evidence and arguments for nonobviousness and conclude that the claimed invention encompassed by appealed claims 1-28, 44-63, and 79-105 would have been obvious under 35 U.S.C. § 103(a).

VII. DECISION

We affirm the obviousness rejections of claims 1-28, 44-63, and 79-105 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136 (a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc

HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 200
TROY, MI 48098